An Analog VLSI Massively Parallel Module for Low-level Cortical Processing in Machine Vision

Giacomo M. Bisio, Melchiorre Bruccoleri, Paolo Cusinato, Luigi Raffo*, Silvio P. Sabatini

Department of Biophysical and Electronic Engineering

University of Genova-Via Opera Pia 11/A-16145 Genova-ITALY

ph: +39 10 3532163, fax: +39 10 3532795, e_mail: silvio@dibe.unige.it

*Istituto di Elettrotecnica - University of Cagliari

Piazza d'Armi- 09123 Cagliari-ITALY

ph: +39 70 281342 (318), fax: +39 70 291619, e_mail: luigi@elettro1.unica.it

Abstract

A new approach to analog VLSI implementations of algorithms for visual cortical processing is presented. Specifically, we introduce a massively parallel architecture, organized as a planar resistive network with voltage controlled current generators locally connected to model interaction schemata responsible of specific sensitivities in cortical neurons. We demonstrate the feasibility of this approach by designing and simulating a 24×24 *nodes analog module implementing Gabor-like oriented receptive fields, that can be used in machine vision real time systems to evidence texture differences.*

1 Introduction

Visual information is processed in a number of successive stages. In mammals, ascending the visual pathway, more and more complex functions are performed, going from luminous contrast sensitivity, in the retina, up to symbolic information extraction, in the visual cortex. Cortical neurons exhibit sharp sensitivity to microstructures in an image, such as simple oriented edges located in a particular region of the visual field as well as more complex features (e.g., gratings) and even extremely complex high-level features, like hands or faces. Consequently, the visual cortex is progressively becoming a fruitful source of inspiration for designing algorithms and architectures in the field of vision processes at low-to-intermediate level. The signal processing capabilities of neurons in visual cortex are characterized by their receptive fields. The pattern of activity that best activates a response of a cortical cell is called its *trigger feature*. The area of the visual field in which this pattern best elicits the neural response is called the *receptive field* of the cell. Each receptive field covers a portion of the visual space acting as a local spatial filter. The spatial structure of receptive fields is related to their ability to detect characteristics of local visual patterns extracting information both in spatial-frequency domain and in spatial domain. Gabor functions, given by the amplitude modulation of a plane sinusoidal wave by a 2-D Gaussian function, maximize the joint selectivity in both domains [1]. Gabor functions are very similar in shape to visual cortex receptive fields [2]. In [3], it has been demostrated that Gabor-like functionalities can be obtained by linear inhibitory interactions of regular distribuited cells that perform simpler operations on the input image (like convolutions with oriented Gaussians).

The possibility of extracting information from images in real time is a keypoint in machine vision systems. Thus, analog hardware devices, in which computation is carried out massively in parallel with high efficiency and speed, are of greatest interest. It is well known [4][5][6] that an analog device that performs a Gaussian convolution on sensory input can be realized by a resistive network with a sensor at each node. This structure can be generalized to obtain elongated oriented Gaussians and Gabor-like spatial transfer functions [7][8]. Specifically, a Gabor-like function can be obtained by inhibitory interconnections between cells along a specific orientation.

The innovative architecture presented in this paper, is based on networks of positive resistors in which the inhibitory connections are implemented by current generators controlled by the voltage at nodes

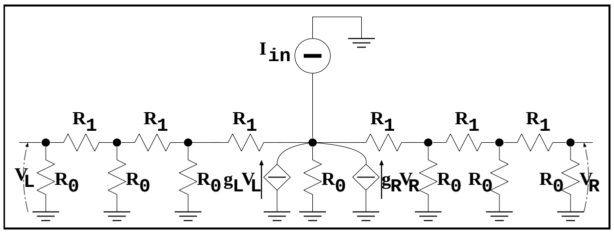

Figure 1: Connections of a node of a 1-D resistive network based on resistors and voltage controlled current generators.

from which the node receives inhibition. This solution allows to consider also inhibitory schema leading to asymmetric convolution kernels, improves stability and simplifies hardware implementation.

2 Analog architecture

Let us consider the functionality of planar resistive networks implementing Gaussian transfer functions [6], and observe that to obtain Gabor-like functionalities it is sufficient to introduce inhibitory connections implemented by voltage controlled current sources. Figure 1 shows a possible schema for the connections of a node in a one-dimensional Gabor-like network. Similar schemata occurs for 2-D networks.

Two main primitives have to be implemented on VLSI neural hardware (resistor and voltage controlled current source). The resistors are directly implemented by high resistivity polysilicon (HIPO), while a specific analog cell has been designed for the other primitive. Figure 2(a) shows a block diagram of the VCCS. It is based on a positive current conveyor [9] that directly supplies or draws current from the node considered. In the current conveyor circuit the opamp acts both as a voltage follower and as a current source, that carries current between two ports at extremely different impedance levels. Specifically, the voltage follower is implemented with a Miller (AB class) transconductance schema. To reduce the number of VCCS for each node a single VCCS is used under the control of the algebraic sum (weighted if necessary) of the driving voltages; for simple cases (e.g. $g_L = g_R$) this operation can be implemented by a small range adder (see Figure 2(b)). The inhibitory voltages V_L and V_R control the two current generators whose total current determines the output voltage (i.e. the control voltage for the VCCS), depending on the value of the CMOS linear resistor [10]. V_c is an externally controlled voltage common to all node-cells, that allows to properly bias the output voltage of the adder.

3 Circuital implementation

A. Component characteristics We assume that the maximum input current coming from the input sensory stage is $30\mu A$. Technological considerations suggest the use of resistors of magnitude in the range of $2K\Omega \div 50K\Omega$ thus implying, for the resistive network configurations considered in this paper, a node voltage range from -300mV to 300mV. The voltage supply of the circuit is a single 5 V, used as a dual 2.5 V supply, by setting the virtual ground to 2.5 V.

In Figure 3 the output current of the voltage controlled current source (VCCS) versus the value of V_R (V_L), when V_L (V_R) is kept fixed. It is worth noticing that the linearity is good in the range showed, that we consider the range in which to optimize the results) the linearity is good. Simulations on the behavior of the VCCS when the load changes show negligible effect.

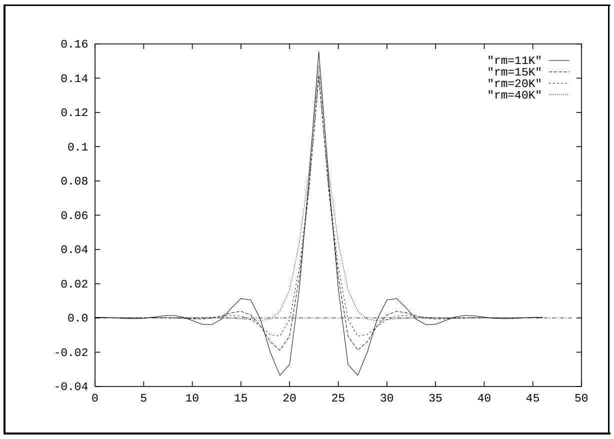

Figure 4: Voltage distribution in a 1-D 47-node network, where $g_R = g_L = 1/r_m$ with r_m varying in the range $11K\Omega \div 40K\Omega$, $R_0 = 30K\Omega$ and $R_1 = 5K\Omega$, when a constant current of $30\mu A$ in injected in the central node.

B. Overall functionality For evaluating the functionality of our circuit solution at system level, we run SPICE simulations both of 1-D and 2-D networks. In Figure 4 the voltage distributions at nodes for a 1-D network (with the schema of connections depicted in Figure 1) is represented for different values of transconductance of the VCCS (i.e. R_{ref} in Figure 2(a)). Comparing circuital and algorithmic solutions it can be observed that the algorithmic kernel is

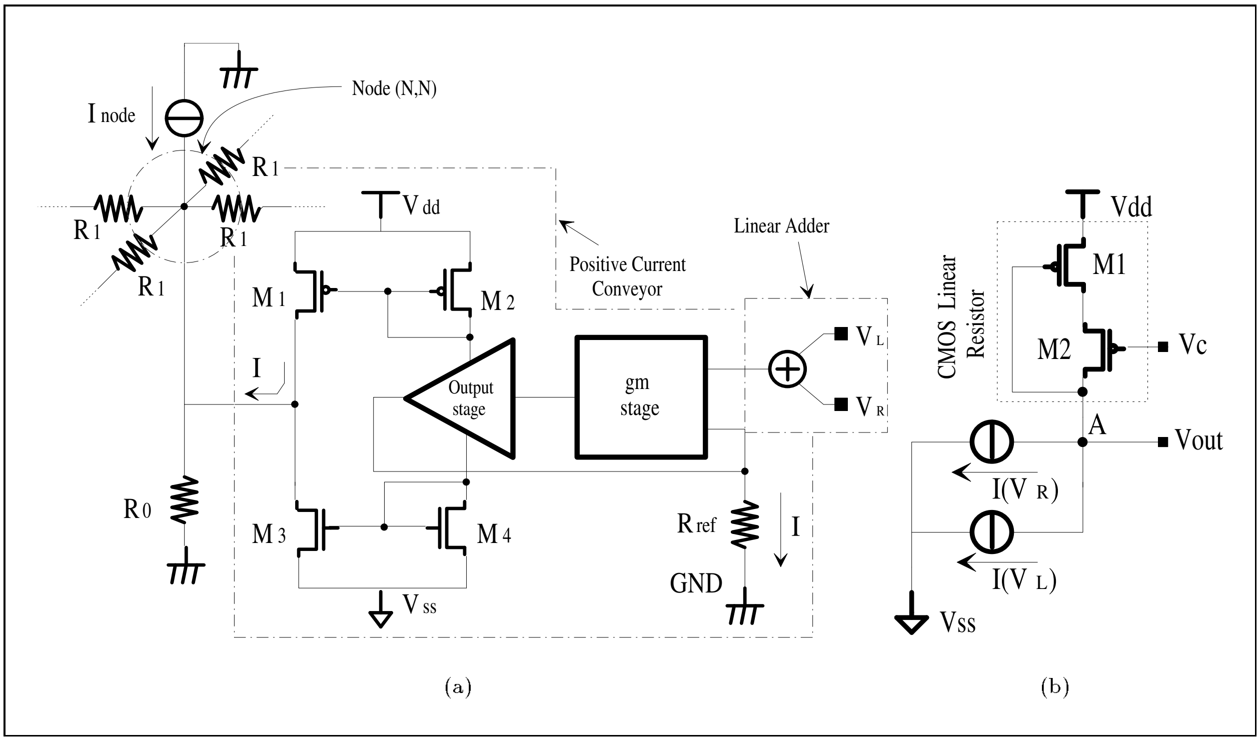

Figure 2: (a)Circuital architecture of a node of a 2-D network. The positive current conveyor implements the voltage controlled current generator. (b)Schema of the small range adder

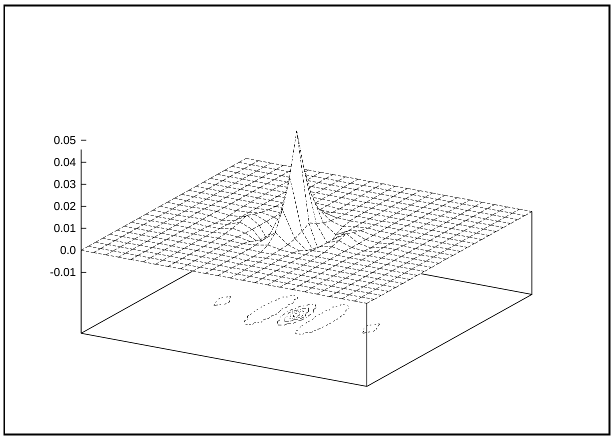

Figure 5: Voltage distribution at nodes of the 24×24 cell module when a $30\mu A$ current is injected in the central node.

number of nodes (pixels)	24×24
technology	MIETEC $2.4\mu m$ CMOS dp dm
number of transistors	13000
number of trans/node	22
node area	$180 \times 165\mu m^2$
power supply voltage	single 5V
power consumption/pixel	$170\mu W \div 460\mu W$
total power consumption	$140mW \div 300mW$

Table 1: Main characteristics of the 24×24 analog cell cortical module

well reproduced by the circuit solution, even though the same response is observed for a transconductance value slightly higher.

C. Cortical Module We have designed and simulated a (24×24) cell module, without on-chip sensors. The module performs the convolution between the image and a Gabor-like oriented kernel, whose orientation can be externally programmed (the choice is among 4 orientations). In this module the inhibitory connection range (the distance between a node and the ones that control the VCCS) is two. Figure 5 shows the voltage distribution when a constant current is injected in the central node. To reduce the single node area and power consumption, particular care has been devoted both to the choice of the analog technology

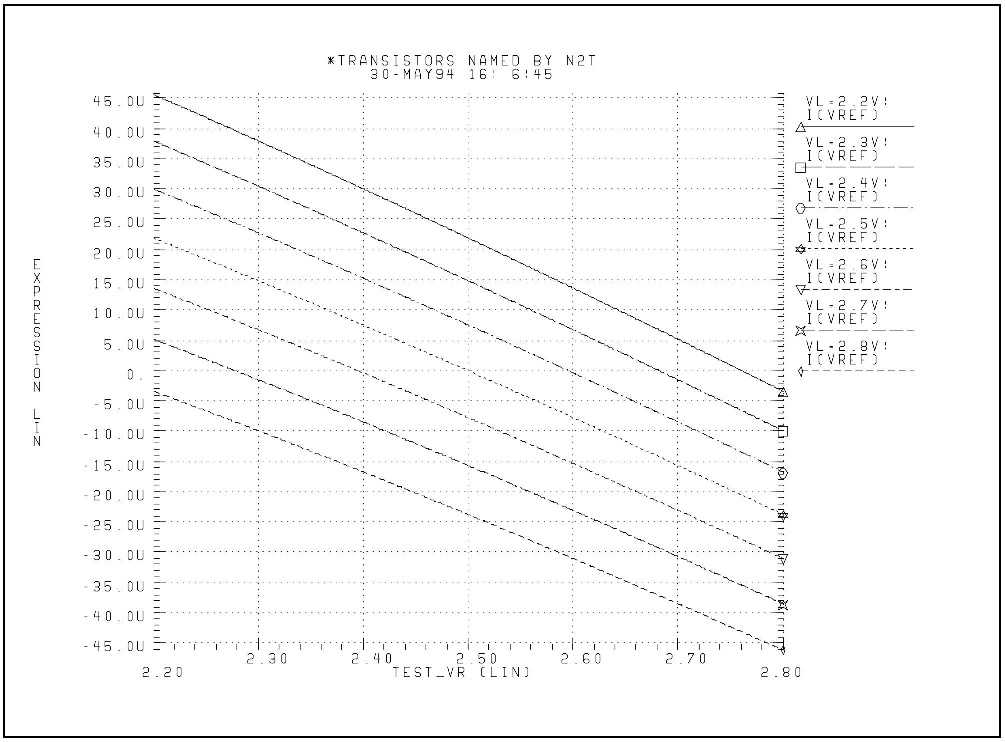

Figure 3: Output current of the VCCS versus the value of V_R (V_L), for different values of V_L (V_R) in the operating range $2.5 \pm 0.3V$.

(low noise and good precision) and to the cell complexity. In this way, with only 22 transistors for each cell, a sufficient level of precision (8 bits of precision) was achieved.Table 1 summarizes the main characteristics of the cortical module.

4 Conclusion

We have demonstrated the analog VLSI feasibility of complex resistive networks emulating cortical processing. Specifically a 24×24 cell module has been designed achieving an accurate implementation of Gabor-like receptive fields, to be used in texture analysis. Along these lines, using asymmetric interaction schemata (i.e. $g_R \neq g_L$) it is possible to obtain different convolution kernels, like even and odd Gabor like functions, to improve the capabilities of the resistive module, since both types of operators are often used in multichannel methods [11].

The approach followed in this paper can be framed in the main stream of Resistive Networks for visual tasks as proposed by Carver Mead and his colleagues. The resistive grid can be seen both as a medium whose structure is in many ways similar to neural structures [12] [13], and as the circuit analogue of the discretized forms of machine vision algorithms [5] [14]. However, the main innovative feature of our approach concerns the effort to map into resistive networks neural visual cortical paradigms such as local computation through oriented receptive fields and to improve their selectivity by superimposing inhibitory connections that are not strictly limited to nearest neighbors.

This circuital architecture is the first step toward the realization of a complete resistor/generators network, that implements an *electronic visual cortex* capable of evidencing texture differences, computing depth mapping and optical flow, recovering surface structure and segmenting images.

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